UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/829,136	04/09/2001	Frankie F. Roohparvar	400.017US01	7233

27073 7590 03/30/2004

LEFFERT JAY & POLGLAZE, P.A.
P.O. BOX 581009
MINNEAPOLIS, MN 55458-1009

EXAMINER	
BRITT, CYNTHIA H	

ART UNIT	PAPER NUMBER
2133	3

DATE MAILED: 03/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/829,136	ROOHPARVAR, FRANKIE F.	
	Examiner	Art Unit	
	Cynthia Britt	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-41 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-41 is/are rejected.

7)☒ Claim(s) 16-33 and 38-41 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 09 April 2001 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-41 are presented for examination.

Drawings

The figures 1-3 of the drawings are objected to because they fail to comply with 37 CFR 1.84 (l), (m), and (t). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the method must be shown or the feature(s) canceled from the claim(s). Method drawings are generally presented in flow chart fashion. No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities: The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Independent claims 34, 38 and 41 recite variables, which are not defined. See 35 U.S.C. 112, first paragraph rejection below.

Appropriate correction is required.

Claim Objections

Claims 16-33 and 38-41 are objected to because of the following informalities: 37 CFR 1.83(a) states that the drawings must show every feature of the invention specified in the claims. Therefore, the method must be shown or the feature(s) canceled from the claim(s). Method drawings are generally presented in flow chart fashion. No new matter should be entered.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 34-41 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Independent claims 34, 38 and 41 recite variables, which are not defined.

As per claim 34, it is unclear to the examiner if the "X" in "X-data" line 4, and "X-control" lines 6 and 7 are the same "X". It is also unclear where the "X/Y" recited in line 7 is described or defined. It is also not clear if the "X" in "X-data", "X- control", and "X/Y" are related in any way or if they are the same.

As per claims 38, and 41, the same issue exists for "X/Y" in line 3 of both claims and "X-bits" in line 2 of both claims. "X/Y" is not defined and "X" is not defined. It is also not clear if the "X" in "X-bits", and "X/Y" are related in any way or if they are the same.

Dependent claims 35-37 and 39-40 inherit the 35 U.S.C. 112, first paragraph issues of the independent claims and will not be further examined on the merits.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 28-33 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 28, the term "X" is not defined in the claim, such as "where x is a positive integer greater than 1"

Claims 29-33 inherit the 35 U.S.C. 112, second paragraph issues if the independent claim and may not be further examined on the merits.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 20-24 and 27 32 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 20, in line 5 "prohibiting the test mode" is unclear. For purposes of examination, the examiner will assume that the circuit is prohibited from entering the test mode.

As per claim 21, in lines 3 and 4 the phrase "a high voltage signal is detected on a predetermined address input" is unclear to the examiner as there is no stated relation of the testing with the address input within the claims.

As per claim 22, in line 5 "prohibiting the test mode" is unclear. For purposes of examination, the examiner will assume that the circuit is prohibited from entering the test mode.

As per claim 23, this claim is dependent on claim 22 and inherits the 35 U.S.C. 112, second paragraph issues of the independent claim.

As per claim 24, in lines 2 and 3 the phrase "a high voltage signal is detected on a predetermined address input" is unclear to the examiner as there is no stated relation of the testing with the address input within the claims.

As per claim 27, in line 5 "prohibiting the test mode" is unclear. For purposes of examination, the examiner will assume that the circuit is prohibited from entering the test mode. In lines 7 and 8 the phrase "a high voltage signal is detected on a predetermined address input" is unclear to the examiner as there is no stated relation of the testing with the address input within the claims. In line 9, "the address inputs" is

unclear due to the plural form of the word inputs where above in the claim only a predetermined address input is mentioned.

As per claim 32, in line 5 "prohibiting the test mode" is unclear. For purposes of examination, the examiner will assume that the circuit is prohibited from entering the test mode.

As per claim 33, this claim is dependent on claim 32 and inherits the 35 U.S.C. 112, second paragraph issues of the independent claim.

As per claim 38, in line 7 "prohibiting the test mode" is unclear. For purposes of examination, the examiner will assume that the circuit is prohibited from entering the test mode.

As per claim 39, this claim is dependent on claim 38 and inherits the 35 U.S.C. 112, second paragraph issues of the independent claim.

As per claim 40, in lines 2 and 3 the phrase "a high voltage signal is detected on a predetermined address input" is unclear to the examiner as there is no stated relation of the testing with the address input within the claims.

As per claim 41, in line 7 "prohibiting the test mode" is unclear. For purposes of examination, the examiner will assume that the circuit is prohibited from entering the test mode. In lines 9 and 10 the phrase "a high voltage signal is detected on a predetermined address input" is unclear to the examiner as there is no stated relation of the testing with the address input within the claims.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3 rejected under 35 U.S.C. 102(b) as being anticipated by Roohparvar U.S. Patent No. 5,526,364.

As per claims 1-3, 7-9, 16-18, Roohparvar teaches the claimed circuit for generating test-mode signals for memory which uses both hardware and software protection schemes. The circuit enters a test code by receiving a high voltage at two terminals. The high voltage must remain on at least one of the terminals during the test code process. Otherwise, the circuit is reset. The test code contains test code bits and format code bits. The format code bits are the same for all test codes and distinguish the test codes from commands. (abstract) A high voltage is placed on two or more pins in order to initiate the test mode. The high voltage is detected by detectors, which may be implemented with known detector circuits. Then, the CE signal is brought low and appropriate test mode codes are placed on the I/O lines and into the buffer. The AND gate ensures that both inputs have a high voltage in order initiate the test code process. The output of the AND gate and the CE signal form the inputs to AND gate. Therefore, with both inputs HIGH, one input will be HIGH. When the other input (CE) is also HIGH, the output is HIGH and turns on transistor, which functions as a switch to transfer the I/O signal from the buffer to a test mode code latch. On the high going edge of the CE signal, the test mode code is latched into a test mode code latch. Since two or more

pins must be at high voltage at the same time during the code entry, this affords the hardware protection during entry of the test code. Therefore, two pins are at a high voltage to load the test mode code and then one of the pins is brought to a low voltage to shut off the loading. If WE falls below the second predetermined voltage, latch is reset through the inverter, disabling the test mode. (Figure 1, column 3 lines 7-42)

As per claims 4-5,10-12, 14-15, Roohparvar teaches the codes are preferably of a specific format, therefore reducing the possibility of mistakenly entering test modes. The codes and their format are preferably sufficiently different than regular commands used to issue activities in the chip. The test mode code is typically divided into two groups of bits. The first is a set of bits that have the same value for a set of different test codes. This section of the code is referred to as the format. (Column 4 lines 17-37)

As per claims 19-27, Roohparvar teaches the logic circuit is initially activated by the CE signal, which turns on a transistor and raises the voltage at the input. The CE signal also enables voltage detection through inverter. Once the output of the voltage detector is asserted signifying that WE is a high voltage, so that the both inputs are HIGH, a latch is set to keep the high voltage detectors powered up even if CE toggles or changes value. A NAND gate and inverter form the latch. This ensures that if the CE signal toggles after setting the latch, the internal test mode execute enable signal remains valid as long as WE remains at a high voltage. This latch is reset if the WE signal falls below a predetermined voltage. The codes are preferably of a specific format, therefore reducing the possibility of mistakenly entering test modes. The codes and their format are sufficiently different than regular commands used to issue activities

in the chip. The test mode code is divided into two groups of bits. The first (format) is a set of bits that have the same value for a set of different test codes. The other bits in the code are used to decode the different test modes, this feature not only makes it safer to keep the test mode codes different from the regular commands, it reduces the circuitry needed to decode the different test modes. By having only one detector for the format bits, that portion of the code requires only one decoder, as opposed to one for each code. (Figure 3, column 3 lines 51 through column 4 line 24)

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 7-9,16, and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Akaogi et al. U.S. Patent No. 6,550,028.

As per claims 1-3, 16-17, Akaogi et al. teach that during the Array Vt test mode, an operator, or alternatively an automated test machine, is able to test each flash memory transistor and determine its Vt. This is done by placing the device in an Array Vt test mode which allows the operator to place external voltages directly on the gate input of a particular flash memory transistor and vary that voltage until the transistor turns on. For the memory device, this testing will be performed on each generation and

even each lot of manufactured devices to establish uniformity and locate any problems in the fabrication process. The device itself utilizing internal logic circuits incorporated into the design of the device provides the Array Vt test mode. The voltage is placed on the gate through an external pin of the device that is routed directly into the flash memory banks, during this test mode. The flash memory transistor to be tested is selected by placing its address on the address inputs of the device. If the voltage placed on the gate is greater than the Vt of the selected transistors, the device, will output a logical 1 for the corresponding bit location otherwise it will output a logical 0. Changing the input address to the device tests each transistor. The test mode utilizes the existing read data path of the flash memory device. During the test mode, the user places an address and a test voltage on inputs to the device. This test voltage is routed directly to the gates of the flash memory transistors selected by the address. (Column 4 lines 1-15, column 13 lines 7-50, figure 2)

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 28 and 29 are rejected under 35 U.S.C. 102(b) as being anticipated by Fang et al. U.S. Patent No. 5,802,071.

As per claims 28 and 29, Fang et al teach that the test-mode switching register can receive an external instruction from a test instrument so as to select a test mode. I.e., it can switch to one of the three test modes. Other test modes can be added, if

necessary. The test control circuit is used for controlling the timing of an external instruction transmitted from a test instrument, and such outer instruction will also be sent to a control circuit-II, via a multiplexer. The control circuit-II is used for decoding an instruction and executing a program instruction, as well as sending an output signal to the test instrument, such as a test machine-II, for comparison. (Column 2 line 60, figure 3)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 4-6, 10-12, 13-15, and 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akaogi et al. U.S. Patent No. 6,550,028 in view of Sher et al. U.S. Patent No. 6,154,851.

As per claims 4, 10, 11, 13-15, 18 and Akaogi et al. substantially teach the claimed memory and method such that during the Array Vt test mode, an operator, or alternatively an automated test machine, is able to test each flash memory transistor and determine its Vt. This is done by placing the device in an Array Vt test mode which allows the operator to place external voltages directly on the gate input of a particular flash memory transistor and vary that voltage until the transistor turns on. For the memory device, this testing will be performed on each generation and even each lot of manufactured devices to establish uniformity and locate any problems in the fabrication process. The device itself utilizing internal logic circuits incorporated into the design of the device provides the Array Vt test mode. The voltage is placed on the gate through an external pin of the device that is routed directly into the flash memory banks, during this test mode. The flash memory transistor to be tested is selected by placing its address on the address inputs of the device. If the voltage placed on the gate is greater than the Vt of the selected transistors, the device, will output a logical 1 for the corresponding bit location otherwise it will output a logical 0. Changing the input address to the device tests each transistor. The test mode utilizes the existing read data path of the flash memory device. During the test mode, the user places an address and a test voltage on inputs to the device. This test voltage is routed directly to the gates of the flash memory transistors selected by the address. (Column 4 lines 1-15, column 13 lines 7-50, figure 2) Not explicitly disclosed is the use of an electronic key.

However, in an analogous art, Sher et al. teach receiving a key to a memory device. A key is conventionally a normally unused combination or sequence of control

signals which may be used to specify or initiate an operation to be employed. A memory device may be a memory integrated circuit (chip) or a memory module. The memory device may be put into a mode with a key. It may be first necessary to unlock the memory device prior to putting it into the mode. By unlock, it is meant that the memory device is taken out of its normal mode of operation. A key may be used to unlock the memory device. Normal memory modes are those used for reading or writing data to a memory array. Such normal memory modes are well known with respect to computer operation. Special modes may be a test mode to test the memory device, or a programmed mode programmed into the memory device which is activated for a preprogrammed operation of the memory device. During the preprogrammed or preconfigured mode, the memory device is read for availability of one or more redundant elements. Column 2 lines 5-39 Therefore it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have used the key taught by Sher et al. with the memory test of Akaogi et al. This would have been obvious as suggested by Sher et al. column 2 lines 12-20 by placing memory devices in modes which are well known.

As per claim, 5, Sher et al. teach a test key approach where transitions of signals at specified times may be used. A test key is provided on DQ1-DQn pins to memory. The test key causes a portion of memory to be put into a programming mode, for which case a programming voltage enable signal transitions from inactive low to active high at a time to enable programming. A programming voltage may be generated with voltage pumps internal to a memory chip to be repaired. A programming voltage may be

supplied by an external voltage source to a no connect pin of the memory device. Programmable elements may include EEPROM cells, antifuses, and the like. (Column 5 line 62 through column 6 line 18 FIG. 1, 5, 6, and 10)

As per claims 6, 12 and 19 Sher et al., teach code(s) or address(es) that may be supplied to the portion of memory via DQ1-DQn. Alternatively, address pins (shown in FIG. 4) may be used for supplying one or more addresses (column 6 lines 21-29).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

"*A High-Speed Parallel Sensing Scheme for Multi-level Non-volatile Memories*" Calligaro et al.1997 International Workshop on Memory Technology, Design and Testing Proceedings, pp.: 96-101

This paper teaches a parallel sensing scheme for multi-level non-volatile memories (ML NVM). A single comparison step is used to achieve high sensing speed. To this purpose, a high-speed low-voltage current comparator is used. Experimental evaluations on a 0.6-μm EPROM test chip demonstrated the feasibility of 4-level-cell NV MLMs from the sensing standpoint. A read throughput of 12 MB/s is achieved with the proposed 4-level-cell memory architecture. Multi-level storage is achieved by using a program-verified scheme to obtain tight cell threshold voltage distribution.

U.S. Patent No. 5,057,715 Larsen et al.

This patent describes a CMOS output driver circuit which has a low threshold device coupled in series between the p-channel transistor and the output terminal. The low threshold device has a threshold voltage (VT) of approximately zero volts. Under normal CMOS driver operation the low threshold device drops essentially zero volts, so that the voltage present at the output terminal, when the p-channel transistor is conducting, is essentially equivalent to a prior art device not having a low threshold device. During special mode operations, when high voltage is impressed on the output terminal, the low threshold device will conduct as long as the voltage applied at the output terminal is less than Vcc-V.sub.T. However, as soon as the terminal voltage increases beyond Vcc-V.sub.T, the low threshold device stops conducting and decouples the high voltage from the drain of the p-channel transistor. This decoupling effectively prevents the high voltage from being applied at the drain of the p-channel transistor. If the high voltage did reach a value greater than Vcc+V.sub.D, where V.sub.D is the p.sup.+ /n.sup.- diode turn-on voltage at the drain of the p-channel transistor, then the p.sup.+ /n.sup.- junction of the drain to substrate of the p-channel transistor would be forward biased which could result in excessive current being drawn between the drain and substrate of the p-channel transistor causing, a turn on of the PNP parasitic bipolar transistor and causing a latch-up condition.

The examiner would like to suggest that applicant carefully review the content of the claims as it appears that after the 35 U.S.C. 112 issues are cleared up there may be up to five separate inventions included in this application. These may be in the

combination – subcombination or subcombination useable together areas. If this is in any way unclear, please contact the examiner at the number below.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 703-308-2391. The examiner can normally be reached on Monday - Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Cynthia Britt
Examiner
Art Unit 2133